# Erasmus Placement Report

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# 1 Introduction

The present report describes the activities performed by the author during his six months period in the Electronic Systems Department of *Vilniaus Gedimino Technikos Universitetas* in Vilnius, Lithuania, under the supervision of Professor Dalius Navakauskas.

The research internship was financed by the Università degli Studi di Verona under the funding of the category D of the Erasmus Placement program and had validation from April 1st to September 31st, 2014.

The objectives set for the period consisted to study the FPGA platform and VHDL, to implement MP systems as digital circuits and to establish a formal equivalence between these systems; with the assistance of the the team led by Prof. Navakauskas and given the extensive history in the design of digital circuits with biological inspiration as also in bioinformatics projects, reason that has driven the author to visit the institution, the tasks were successfully performed as described in the body of this report.

Additionally, since the project developed is part of the author's doctorate research, it has been strongly benefited by a series insights and results produced in the period.

# 2 Developed Activities

In the period spent in the research internship at VGTU, a considerable quantity of activities were developed. The duration of the them depends on factors such as its complexity, the familiarity of the researchers with the topic in consideration, availability of resources, among others; hence, one should not be surprised neither by the quantity nor the length of the them and, actually, may infer the amount of work necessary to complete each of them.

It has been chosen to list the activities in the chronological; this way, the reader can immerse in to the challenges faced as well as the reasoning and work fluxes of the author in his period of the research internship.

Another unorthodox definition is the time scale used to report the activities: although the highest precision would be desired, a monthly scale is accurate enough and transmits the real difficulties in performing the tasks.

## 2.1 Study on VHDL

As previously accorded in the training agreement, the investigation on MP systems and digital circuits was guided by implementations on Field Programmable Gate Arrays (FPGAs) using the VHSIC (Very High Speed Integrated Circuits) Hardware Description Language (VHDL). VHDL can be seen as an analogous to programming languages for digital hardware implementation in which one can describe the design not only by its electronic components but also by its behavior through stepwise declaration of assignments to signals, including operations over values and function application.

Although it is influenced by programming languages, its syntax is considerably different; given the loose restrictions of a circuitry interaction with the environment, VHDL presents features for dealing with synchronization and modification of signals, for example, that are absent in most of the programming paradigms. These discrepancies, hence, requires special training for a newcomer.

This way, in the whole month of April, the efforts were concentrated in acquire the sufficient knowledge on VHDL and the details to port projects to the target board for implementation, the Digilent Nexus V3.

The main literature was Pedroni's "Circuit Design with VHDL" [14], followed by Ashenden's [2], Spiegel's [20] and Chu's [4] texts; some review on digital systems were supported by Tocci [23] and the details of fixed-point arithmetic was learned through technical reports [3, 11].

Even more useful, though, was the support given by the PhD candidate Tomyslav Sledevič, from which both altruism and expertise in the hardware description language and the target board saved efforts from the author in the learning process; it is his merit for the complete environment bootstrap as well as the clarification over synchronization questions.

## 2.2 Study on Digital Circuits

It is difficult to clearly understand VHDL without the supportive knowledge on design of digital circuits: the latter is not only related to the final product which is developed, but also drives the project decisions

on all levels, from the type of signals to choices of algebraic operations to be used in the design to time synchronization of modules to the architecture of the designed circuit.

In the current project, several challenges involving the theory of digital circuits design were present; to name a few, it included the representation of rational numbers (float-point, fixed-point or scaling), minimization of the number of used components, definition of combinatorial and sequential circuits, modeling languages of digital circuits (Boolean algebra, finite state machines [7, 9], block diagrams [12], signal flow graph [8], dynamical systems [7]) among others.

For this reason, in the months of April and May, studies on digital circuits design were performed in parallel with other activities. In the first moment, it occurred sporadically in support to VHDL study or hardware description work; later, however, it took a central importance when the attempt of a theoretical correlation between MP systems and digital circuits.

As the bibliography used, mainly it was the Tocci's "Digital Systems: Principles and Applications" [23], followed by some excerpts of Peroni [14] and, on modeling languages, by the aforementioned books [7,9,12].

## 2.3 BISIP 2014

As a part of a research internship, Prof. Navakauskas has stimulated not only the development of digital circuits and final results of the proposed research, but also has spanned its influence and expertise to other ones; the attendance at the *The 3rd IEEE Workshop on Bio-Inspired Signal and Image Processing (BISIP 2014)* was the first of these examples.

The workshop is an effort of both Lithuanian and Polish chapters of the IEEE to present, discuss and interconnect researches with focus on biological application or those who imitates observed biological behaviours. Its second edition, in which the author participated as a spectator, took place in the Electronic Department of VGTU in Vilnius, Lithuania, at May 5th, 2014 and presented an invited lecture and eight submitted presentations.

Although not directly correlated with the project of the internship, some of the presentations indirectly contributed to the evolution of it; for instance, Mr. Sledevič's "Hardware Implementation of Isolated Word Recognizer", in which he presents the challenges in the implementation of a word recognizer in FPGA.

## 2.4 Implementation of MP models in VHDL

After a month of studying the VHDL description language and architectures of digital circuits, the implementation of MP models in VHDL started. One month ahead the original planning in the training agreement, it had a calm start with attempts to understand all the relationship between the MP internals and VHDL primitives in order to progress in the development without obstacles.

This activity can be divided, for didactical purposes, in three main parts: (i) study of a general translation of MP systems to VHDL representation; (ii) implementation of VHDL source code; (iii) cyclic iteration of debugging. These subdivisions occurred in a semi-parallel, overlapped schedule and they are strongly interdependent; this way, it is very difficult to measure the amount of resource each of them has consumed individually. Then, it is said that, altogether, they have intensively consumed the second half of April and May, but with recurrent review in the following months.

### 2.4.1 MP systems and VHDL primitives

A valid strategy to understand the correlation between MP systems and VHDL is trying to find out how primitives of VHDL—*i.e.*, the building blocks of the description languages—are used to model a (generic) MP system. For this, both representations are decomposed in modules to then search for a way to model one based on the other.

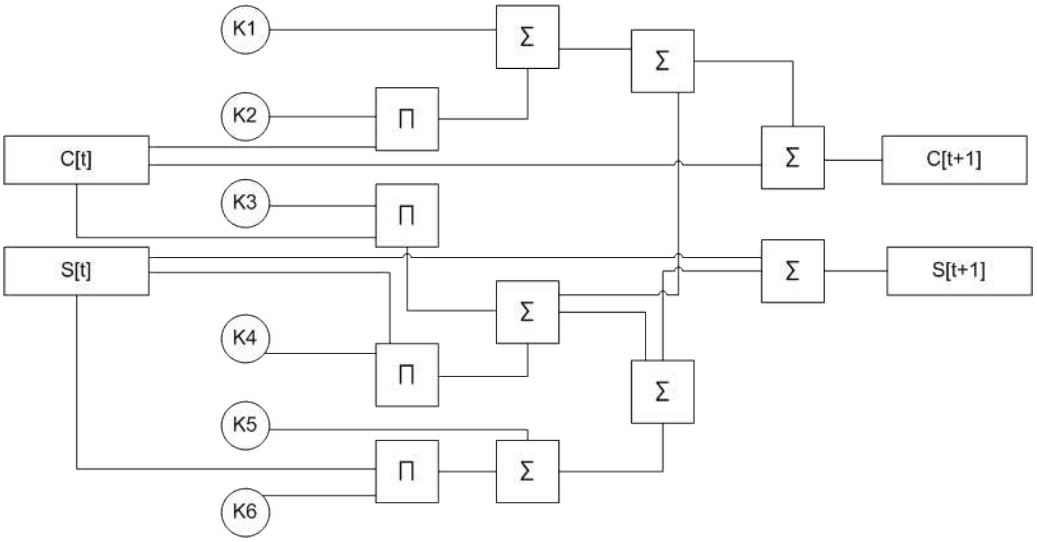
Although theoretically it sounds simple and the organization of MP systems in well-defined rules may be seen as an advantage for this approach, the loose restrictions on the expression of the fluxes of each MP rule that poses as a obstacle for this simple analysis procedure; since any computable function [9, 19, Definition 5.17; Definition 4.2.3] can be used to compose the flux formulæ, the basic arithmetical operations (as VHDL primitives and basic digital circuit modules) stop being enough for representing more than the basic systems and additional subsystems, such as intermediary memory units, are required.

This complicating factor let to the development of the idea of architectures of MP systems that could describe the general structure of a system through a network of modules, each one responsible for a particular activity of the system's processing procedure.

Using an approach influenced by the studies of compiler theory [1], register-transfer level (RTL) synthesis and systems theory [12], an arithmetical network (see Figure 1) was established to completely

represent a MP system as a the feedback loop on its variables and its composing rules and fluxes using box diagram as an intermediate modelling language between MP systems (or, precisely, MP graphs) and digital circuit representation.

Figure 1: Arithmetical network for the Goniometricus MP system.




This new representation presents a series of advantages over the preceding ones in the present context: (i) it is similar to the block diagrams and signal-flow graphs used in control theory [12, Chapter 3], approximating this field to MP; (ii) it specifics the arithmetical operators in use, which there are direct translations to circuitry modules; (iii) it makes explicit all the signals used (as well as where they are) in the systems modeled; (iv) it is easy to delimited sub-regions such as fluxes and rules and the (final) aggregator of results; (v) it is much the same as a data path from circuits design [24]; (vi) it uses a notation compatible to the standards IEC 60617-12 and IEEE Std 91; and last, but not the least, (vii) it resembles a artificial neural network, a field of intensive studies in computer science, by the group of Prof. Navakauskas at VGTU and in recurrent discussions in the Prof. Manca's group.

### 2.4.2 Implementation of VHDL code

Coding a VHDL implementation was a straightforward activity after (and while) the study of the details of MP systems and its translation to digital circuits, specially the activity report in § 2.4.1. In fact, the translation of the classical MP rules into VHDL code was, almost, *ipsis litteris*, except by some required signal length manipulation in order to keep them typologically equivalent.

Most of the effort on the implementation activity, nonetheless, in two activities: proofs-of-concept using different arithmetical representations (float-point, fixed-point and scaling, as described in § 2.2) and debugging the code to resolve diagnosed problems. As expected, these are deeply related since value rounding and error propagation in computation were the most common problems.

Listing 1: A sample of the VHDL code for the Goniometricus dynamics.

```
architecture dynamics of bookGoniometricus is
    -- components
    component frequencyDivider is
        port (
            rawSignal   : in std_logic;
            divideBy    : in natural range 1 to natural'high;
            newSignal   : out std_logic
        );
    end component;

    -- functions

    -- signals and variables
    signal should_run   : std_logic := '0';
```

```
    signal step_clock : std_logic := '0';
begin
    -- port maps
    updateValue: frequencyDivider port map (
        rawSignal   => clockBook,
        divideBy    => 100000,
        newSignal   => step_clock
    );

    -- combinational instructions
    should_run <= run;

    -- sequential instructions
    step: process (step_clock, should_run, resetBook)
        variable rule_1 : ufixed (integer_part_length-1
                                  downto -fractional_part_length);
        variable rule_2 : ufixed (integer_part_length-1
                                  downto -fractional_part_length);
        variable rule_3 : ufixed (integer_part_length-1
                                  downto -fractional_part_length);
        variable cosine_var : ufixed (integer_part_length-1
                                      downto -fractional_part_length);
        variable sine_var : ufixed (integer_part_length-1
                                    downto -fractional_part_length);
    begin
        if (rising_edge(step_clock) and should_run = '1') then
            if (resetBook = '1') then
                cosine <= cosine_zero;
                sine <= sine_zero;
            else
                rule_1 := resize(k1 + resize(k2 * cosine, rule_1), rule_1);
                rule_2 := resize(resize(k3 * cosine, rule_2) +
                          resize(k4 * sine, rule_2), rule_2);
                rule_3 := resize(k5 + resize(k6 * sine, rule_3'high, rule_3'low),
                                 rule_3);
                cosine_var  := resize(cosine + rule_1 - rule_2, cosine);
                sine_var    := resize(sine + rule_2 - rule_3, sine);
                cosine <= cosine_var;
                sine <= sine_var;
            end if;
        end if;
    end process step;
end dynamics;
```

## 2.5 Search for the Equivalence Between the MP and Digital Circuits Models

Few examples of MP dynamics implemented as digital circuits, although an original result that produces insight for improving the research field, are not enough to justify the generality of the equivalence between the models. It is expected, therefore, a formal (and, by natural consequence, theoretical), general and correct proof of the equivalence to extinguish any questions or obstructions concerning the usage of this equivalence in future applications.

Given its important, from the end of May to the month of August, the author has been deeply involved to the seek of the proper equivalence result between MP systems and digital circuits through a number of investigations on mathematical and engineering concepts, which defined a series of nested smaller activities.

It is relevant to anticipate that although complete result has been achieved, important landmarks has been reached and the research track is well-defined and established and the on-hold period is justified by the present lack of collaboration from other fields, such as abstract algebra and category theory.

**MP and Arithmetical Network** As described in § 2.4.1, arithmetical networks were developed under the influence of several fields in order to explicit the interconnection of signals in MP dynamics. This

new modeling technique has made clear the interdependence of the signals and the necessity of additional information, such as memorized signals.

**MP and Combinational Circuits** Combinational circuits are those that work under the rules of combinational logic, *i.e.*the processed output of the circuit do not depend of time-dependent information; in other words, a combinational circuit is a function depending uniquely on its input, which time does not belong to. For instance, a Boolean network implemented through logic gates is a representative of this kind of circuit; arithmetic operations such as addition or multiplication are also instances of combinatorial circuits and, as the components of the arithmetical networks of MP dynamics, they were the trigger to the study of the relation between MP systems and combinational circuits.

The end of May and first days of June was dedicated to this study that has not gone long: when the general equivalence between MP systems and feedback ones were noticed, it became clear that purely combinatorial circuits are not enough [14, § 5.1].

**MP and Sequential Circuits** Then, in the first half of June, a study on sequential circuits and its possible equivalence to MP systems was undertaken. In opposition to the combinatorial circuits, sequential circuits depend on the input data and time or, in other others, its output depends on previous inputs [14, § 5.1] and, hence, depends on memory units.

Although more complex than combinatorial ones, sequential circuits are more expressive than its counterparts; feedback systems, for example, can be implemented using this kind of circuit [14, § 5.1]. Also, its is widely known they representation as dynamical systems and, particularly, finite state machines [7, § 1.5, § 1.5.2 and § 2.1.6], both subjects associated to MP in its formal definition as the special case of the former [10, § 3.1] or by latter expression of software [25] and the software-hardware equivalence [22, 26].

Since sequential circuits (finite state machines and automata) are special cases of dynamical systems, the amount of formal studies over the latter is bigger (which include properties analysis and decomposition in classes) as well as closer MP to its notation, this study naturally transitioned under the dynamical systems theoretical.

**MP and Sequential Circuits as Dynamical Systems** The common language of dynamical systems for representing both MP systems and digital (sequential) circuits brings a series of advantages to the pursuit of the equivalence between these two models. Among them, one can cite the extensive literature on the subject, the application of the same definitions and results and existence of similar problems already solved [7, § 2.4].

During the period of two months and a half (middle June to August) dedicated to this study activity, it was populated by diverse smaller tasks in an attempt to better understand the theoretical content of the both models under the dynamical systems perspective, as well as numerous ventures to mathematically demonstrate the intended equivalence. Because of the exaggerated technical content and unsuccessful outcomes not relevant for this report, these endeavours are briefly enumerate in chronological order:

1. MP and Analog Circuits: middle of July and middle of September;
2. Dynamical Systems as Algebraic Groups, Commutative Diagrams and Category Theory: middle of July and August;
    - Formalization of the Equivalence: August.
3. Tanevski and Prescott perspective to MP: middle of July;
4. Control Theory Perspective: middle of July;
    - Arithmetic Network as Block Diagram and Signal Flow Graph.
5. Synthesizable VHDL instruction set and Group Theory: end of July.

**Work on Equivalence Proof** It is not easy to define a date for the beginning of the work on proving the equivalence between MP systems and digital circuits once, during the studies on dynamical systems as mathematical abstractions, it has started as simple sketches and attempts to fit ideas in a conceptual framework and, soon, naturally evolved to rigorous arguments involving constructions with advanced mathematical knowledge. Hence, it is precise enough to assert the start of the work on the proof in the middle of July, stimulated by ideas from linear systems, and has advanced up to the month

of August, when a document with arguments covering category and abstract algebra theories where sent to other researchers in seek of help to its development; from that moment thus far, however, this activity has been frozen to evaluation of the formal steps and proposal of solutions for the current open problems.

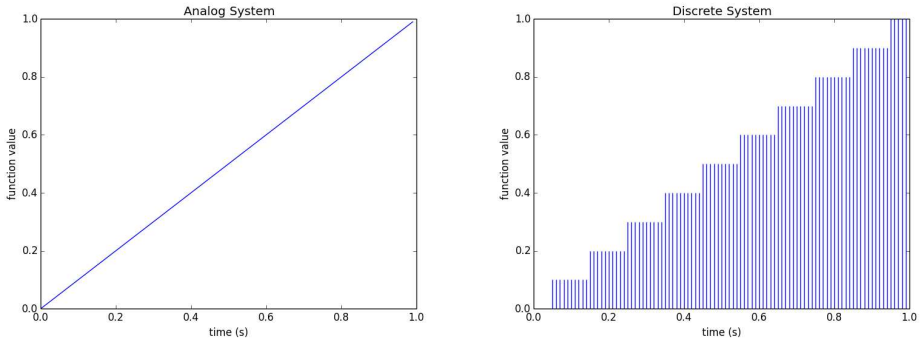
## 2.6 Analog Circuits

Three particular occasions has sparked, in the period of this research internship, the evaluation of MP systems as analog circuits: middle of June, middle of July and middle of September. The interest in these areas has arisen for different reasons, but this kind of circuit is particularly attractive because of its precision to represent quantities [7, § 1.5], its speed in comparison to digital ones or software [21] and its promising properties [13, 16, 18], among others.

The first of the times it has been in a discussion with Prof. Rahul Sarpeshkar and his ideas of symbiosis between analog circuits and biology [16, 17]; in particular, his attempt to model system biology using analog components seemed too complicate to the author and, hence, it has stimulated reflections on MP systems as a substitute for it, as well as a modelling language for analog computation.

Then, in the middle of July, this proposition has again emerged while studying dynamical systems and their dimensional properties. In that moment, the computational power of MP systems and analog systems were confronted, with the outcome that MP systems, as defined in *Infobiotics'* book [10], is strictly less powerful than analog ones because of the discretization of information and its limits of value representation.

Figure 2: Comparison between analog and discrete systems.




The last of these recurrences occurred in September, in a meeting with Prof. Navakauskas and Prof. Gytis Mykolaitis. In the occasion, it has been discussed the techniques used in Prof. Mykolaitis articles to model dynamical systems—for instance, the modelling of FitzHugh-Nagumo oscillators [21]—and how MP systems, which are inherently discrete ones, into analog circuits.

Although exists an interesting in the subject, it has always been outside of the scope of the present research and has been treated as a curiosity and possible future investigation area, with no further efforts been invested on it.

## 2.7 Collaboration in the PhD Description

For a period of a couple of days, in the second half of May, the author has collaborated with Prof. Navakauskas in the composition of a research description for doctorate position funding.

This brief and small activity consisted of gathering some references on bio-inspired engineering related to my current research project and compose a written motivation over the research topic, pointing out the reasons of its relevance for the scientific community through existing research publications.

This activity has been particularly rewarding because it has required an update in the author's knowledge library, served as a tiny preview and writing practice for the present report and, most important, attracted funding and student for the research field.

## 2.8 Lecture on PhD Research

In the date of June 17th, 2014, an IEEE Lithuania Section Seminar Series lecture on the doctorate research project of the author has been held in the Electronics Department of VGTU and organized by the Prof. Navakauskas.

The lecture presented the concepts of MP systems, examples of its application and the road map of the research project, with focus on electronics circuits and their importance as a gateway from MP theory to engineering to synthetic biology; for illustration of the impact of this coupled research, ongoing research projects such as SyNAPSE [5, 6] and Human Brain Project [15] were used.

The electronic and interactive version of the presentation is available online at `http://ricardo.guiraldelli.com/resources/presentations/2014-05-28/2014-05-28.svg`.

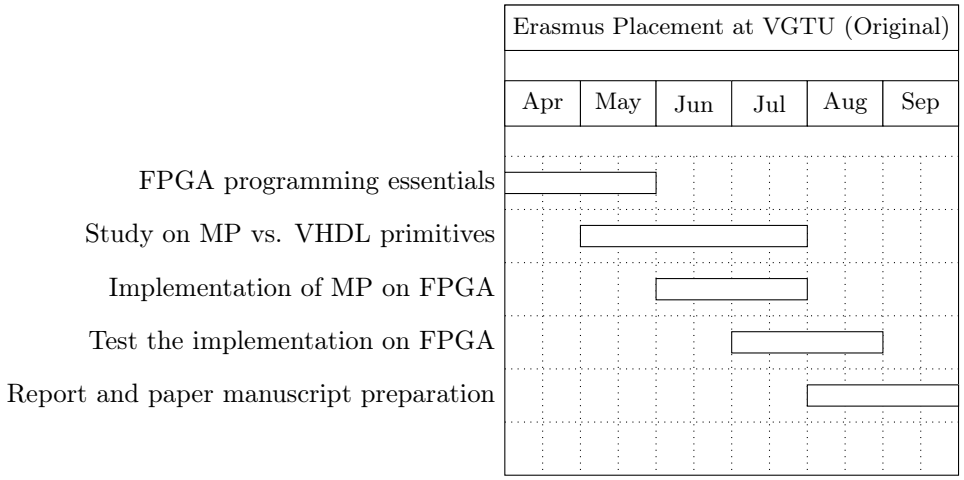
# 3 Unfinished Activities

The original planning for the period was realistic and the activities were well-defined; yet, when the developed activities are compared side-by-side, there is a single one not it finished, namely *technical report and paper manuscript preparation*; although the *technical report* consist of the present document, the *paper manuscript* has yet to be started.

The paper manuscript has been delayed for the production of more results derived from the period abroad, such as digital implementation of a range of dynamics and a partial formal justification of the equivalence between these systems and digital circuits (still in hold, as referred in the § 2.5, ¶ *Work on Equivalence Proof*).

However, given the interest of the research teams both in VGTU and UNIVR, this manuscript is planned to start as soon as the author returns to his original research unit for the composition of a transnational research article, targeting proper conference, in collaboration with Prof. Navakauskas and his group.

Figure 3: Gantt chart of the planned activities for the Erasmus Placement program.




# 4 Conclusions

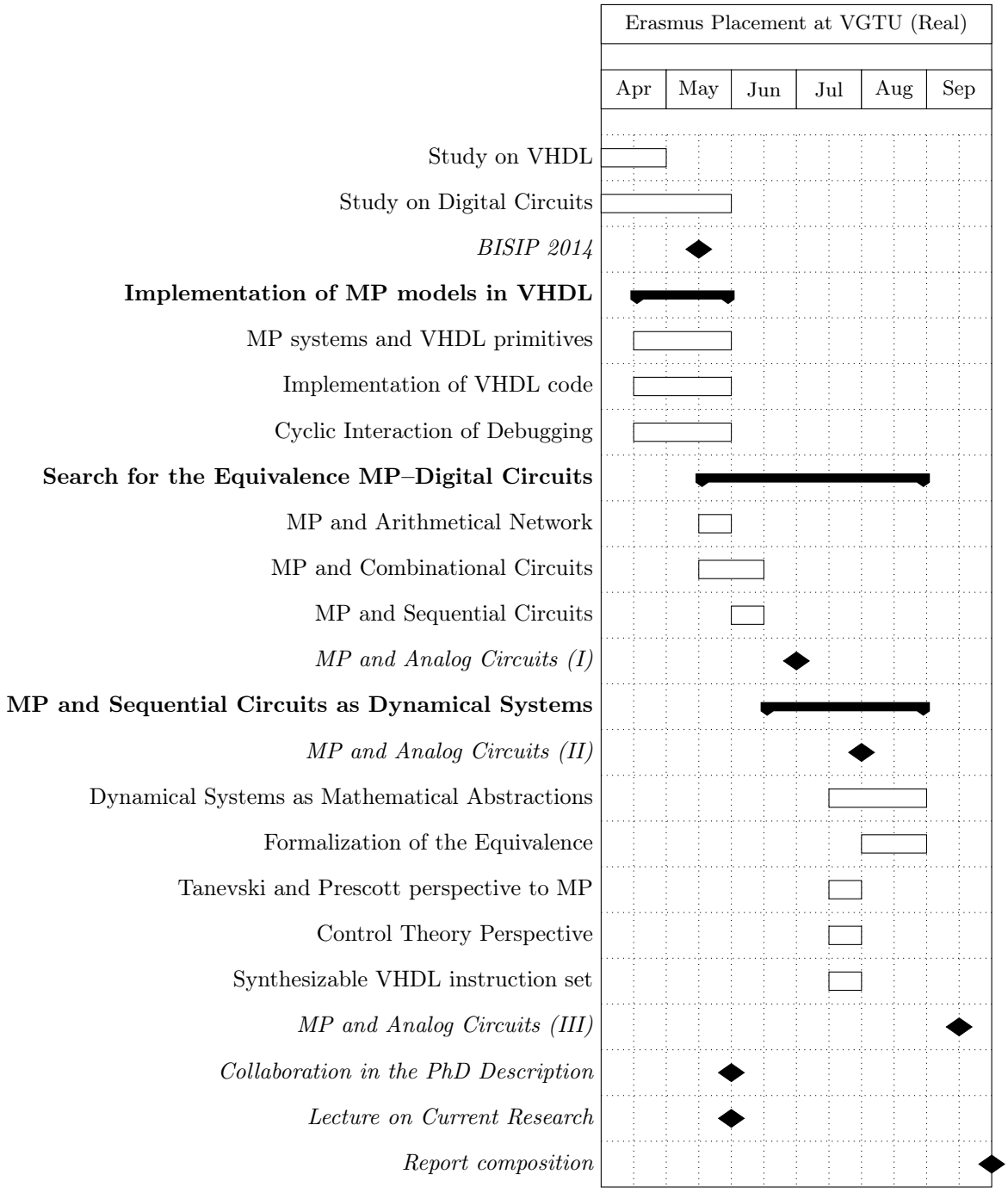
If it was possible to summarize this conclusion to one single word, it would be *productive*; nonetheless, one must justify the choice of the word.

Back to the original research unit, Università degli Studi di Verona, the research on the equivalence of MP systems and electronic circuits is focused on temporal series (dynamics) and the retrieval of their generating rules using the Log-Gain Stoichiometric Stepwise (LGSS) regression algorithm [10, § 3.4] because of the existing know-how of the group. There, questions such as which type of dynamics are possible to express through MP theory or the reasons why a particular set of rules misbehave are promptly answered.

On the other hand, the Verona group lacks knowledge on electronic circuits, what has trapped the current research project in a circle of ideas testing that has prevent further development: analog circuits, digital circuits and fast Fourier analysis were some of the subjects recurrently on study—and with some results produced on the latter one—but little divergent from the proposed research track.

The period at the *Elektroninių Intelektualiųjų Sistemų Grupė* at the *Elektronikos fakultetas* of the *Vilniaus Gedimino Technikos Universitetas*, however, has given a *fresh air* to this research. With their

Figure 4: Gantt chart of the realized activities for the Erasmus Placement program.



well-structure laboratory, availability of devices and personal for experiments and precise research schedule, it was possible to implement MP dynamics in FPGA, observe the generated schematic diagrams, propose a general rule for digital circuit translation of MP systems (through arithmetical networks, as described in § refsec:vhdl-primitives) and start and greatly advance a formal proof of the equivalence between the models—results that, certainly, lay over the extensive knowledge developed in the several trials, experiments and reflections occurred previously in the original research unit.

This way, the six-month period at VGTU was very important to consolidate some of the previously existing ideas and ideals, to experiment and acquire new knowledge and to produce significant results for this interdisciplinary topic. Simply *productive*.

## Acknowledgments

The work presented in this report, although attributed to a single author, is a product of the collaboration of diverse researchers, staff and friends that has spread beyond the walls of the room 413 at 41 Naugarduko street in Vilnius, but will continuously be present and follow this research. Nominally, each collaborator will be acknowledge, but the author's divergent mind may naïvely forget some names: in this case, he apologizes in advance.

At first, the deepest gratitude to Prof. Dalius Navakauskas and his PhD candidate, Mr. Tomyslav Sledevič: they have trusted to a foreigner, unknown and hidden for months behind an email address, great amount of their time, knowledge, research effort, equipment, room and all the resources one could need to properly execute a scientific investigation; their professionalism and tutoring abilities serve as a role-model for the whole scientific community.

Then, in Italy, the sincere appreciation to Prof. Vincenzo Manca and Prof. Gloria Menegaz: their support and careful consideration of my proposed PhD research and Erasmus Placement candidature were essential to this fruitful period abroad from which the results will continue, under their watch, to produce scientific goods.

Back to Vilnius, my thanks to Artūras Serackis, Dalius Matuzevičius, Darius Plonis, Dovilė Kurpytė and Raimond Laptik: their technical and daily-life advices, as well the small talking and laughts, were extremely valuable to the survival of the researcher and its research project.

Outside the laboratory, Justina Pluktaitė and Jelena Mazaj deserve all the credits for keeping the author's calmness in place when the bureaucratic issues has arisen: for this and all the guidance, thank you.

At last, but not least important, the *Lithuanian family* of the author: Eglė Naraškevičiūtė, Jolanta Naraškevičienė, Edvinas Naraškevičius and Jonas Baltrūnas; these were the people that really supported the author's life in Lithuania in all aspects outside the university walls and for which he is long-life grateful: those are his (extended) family members for now and then in both the *Old Continent* and the *Brave New World*.

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